AQA

Please write clearly in block capitals.

Centre number | | | | | | Candidate number | | | | |

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A-level PHYSICS

Paper 3
Section B Electronics

Thursday 14 June 2018 Morning

Time allowed: The total time for both sections of this paper is 2 hours. You are advised to spend approximately 50 minutes on this section.

Materials

For this paper you must have:
- a pencil and a ruler
- a scientific calculator
- a Data and Formulae Booklet.

Instructions
- Use black ink or black ball-point pen.
- Fill in the boxes at the top of this page.
- Answer **all** questions.
- You must answer the questions in the spaces provided. Do not write outside the box around each page or on blank pages.
- Do all rough work in this book. Cross through any work you do not want to be marked.
- Show all your working.

Information
- The marks for questions are shown in brackets.
- The maximum mark for this paper is 35.
- You are expected to use a scientific calculator where appropriate.
- A Data and Formulae Booklet is provided as a loose insert.

For Examiner's Use	
Question	Mark
1	
2	
3	
4	
5	
TOTAL	

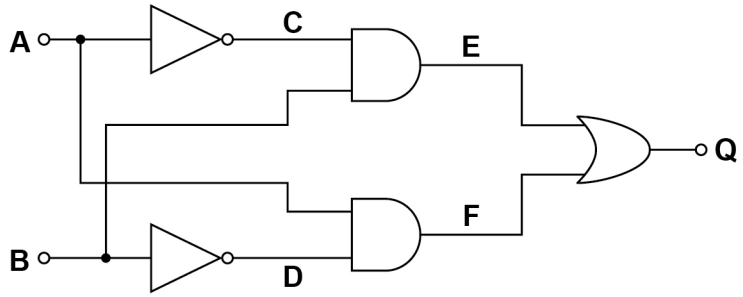
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Section B

Answer **all** questions in this section.

0 1 . 1 Two logic inputs, **A** and **B**, feed into the logic circuit shown in **Figure 1**. The logic output from the circuit is **Q**.

Figure 1



Deduce the Boolean expression for the output of this logic circuit in terms of inputs **A** and **B**.
Include all the logic operations that take place between the inputs and the output.

[2 marks]

Q = _____

0 1 . 2 The truth table shows some of the logic states for the logic gates in **Figure 1**.

Complete the truth table.

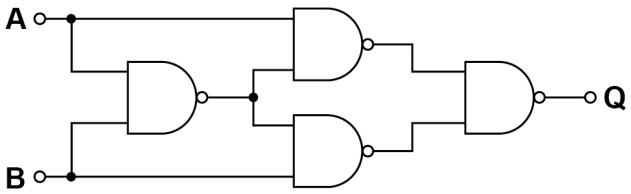
[2 marks]

B	A	C	D	E	F	Q
0	0		1		0	0
0	1		1		1	1
1	0		0		0	1
1	1		0		0	0

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0 1 . 3 **Figure 2** shows a different logic circuit that produces the same logic output as that of **Figure 1**.

Figure 2



A manufacturer wants to produce a system that uses this logic function, but is undecided as to which circuit to use.

Suggest, giving reasons, **two** benefits of using the logic circuit in **Figure 2** compared to the logic circuit in **Figure 1**.

[2 marks]

0 1 . 4 State the single logic gate that would perform the same logic function as the circuits shown in **Figure 1** and **Figure 2**.

[1 mark]

7

Turn over for the next question

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0 2 . 1 An ultrasound sensor produces an output that needs to be amplified to $3.0\ \text{V}$
The amplifier used has a voltage gain of 40

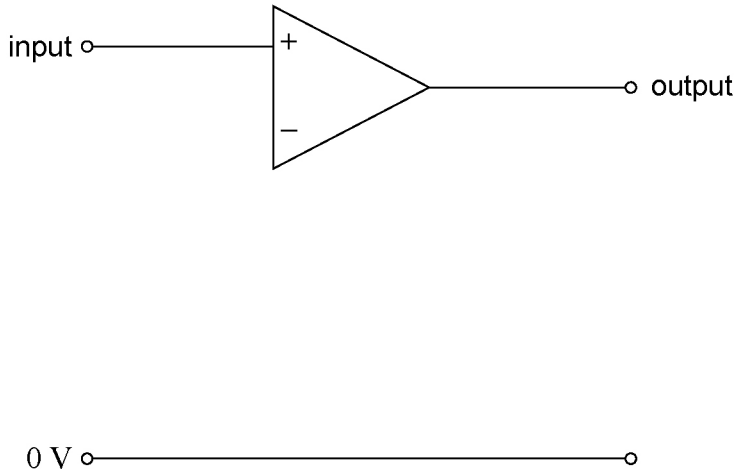
Calculate the input voltage V_{in} to the amplifier from the sensor.

[1 mark]

V_{in} = _____ V

0 2 . 2 An operational amplifier in non-inverting mode is used to amplify the output of the sensor. The partially completed circuit diagram is shown in **Figure 3**.

Figure 3



Complete the circuit diagram in **Figure 3** by adding and labelling two resistors, $\boldsymbol{R}_{\text{in}}$ and $\boldsymbol{R}_{\text{f}}$, so that the operational amplifier is correctly configured in its non-inverting mode.
The power lines should not be shown in the completed diagram.

[2 marks]

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0 2 . 3 Determine, using resistors selected from the list below, how the voltage gain of 40 can be achieved by the non-inverting amplifier of **Figure 3**.

1 kΩ 3.6 kΩ 10 kΩ 39 kΩ 150 kΩ

[2 marks]

R_{in} = _____ kΩ

R_f = _____ kΩ

0 2 . 4 The ultrasound frequency detected by the sensor is 50 kHz
For this operational amplifier

gain × bandwidth = 1.0 MHz

Discuss whether this operational amplifier is suitable for amplifying the sensor's output voltage.

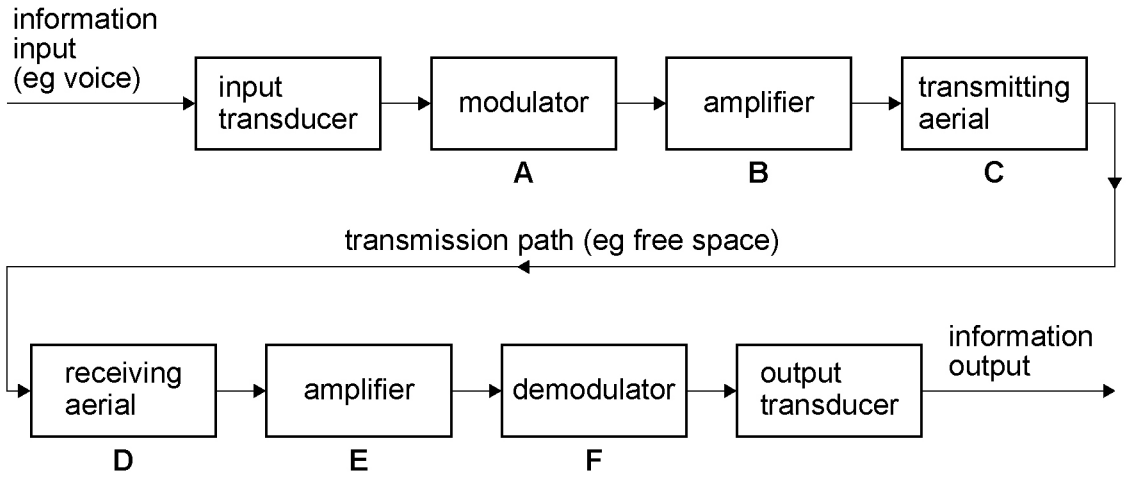
[2 marks]

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0 3 **Figure 4** shows a block (subsystem) diagram for a radio communication system.

Figure 4



0 3 . 1 State the letter representing the subsystem in which you might find an induced emf being generated.

[1 mark]

0 3 . 2 State the letter representing the subsystem where the audio and radio waves are combined.

[1 mark]

0 3 . 3 The signal strength at stage **D** must be amplified.

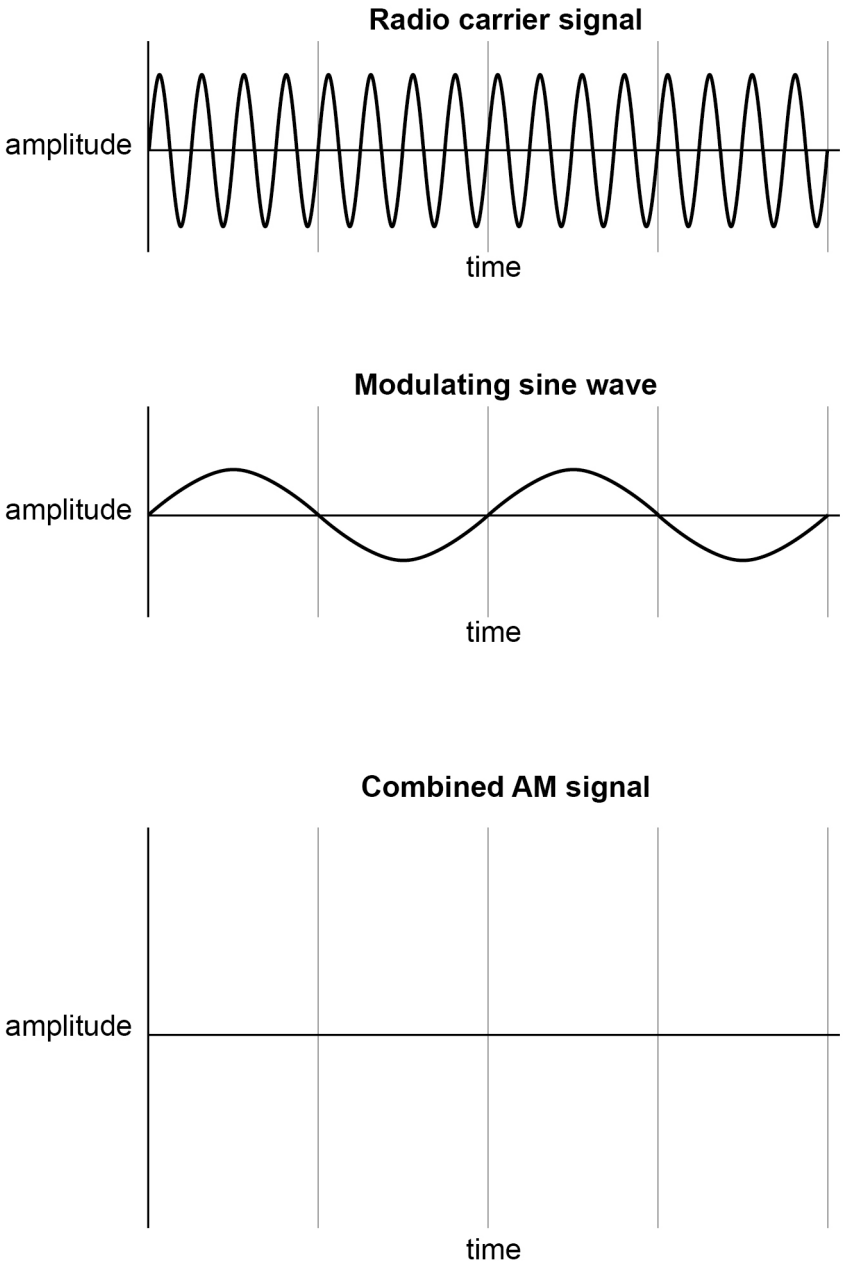
Explain why the signal strength at stage **D** is weak.

[1 mark]

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0 3 . 4 **Figure 5** shows graphs of a radio carrier signal and a modulating sine wave.

Figure 5



Complete the graph in **Figure 5** to represent the combined amplitude modulated (AM) signal.

[1 mark]

Question 3 continues on the next page

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0 3 . 5 Approximately 20 radio stations use amplitude modulation (AM) to broadcast to people living in the London area. Another 35 AM stations broadcast to people outside the London area. However, these broadcasts can still be received in London.

The allocated frequency spectrum for all these broadcasts is in the range 540 kHz to 1600 kHz

Suggest whether all these stations can broadcast hi-fi music using the full audio frequency of 20 kHz

[3 marks]

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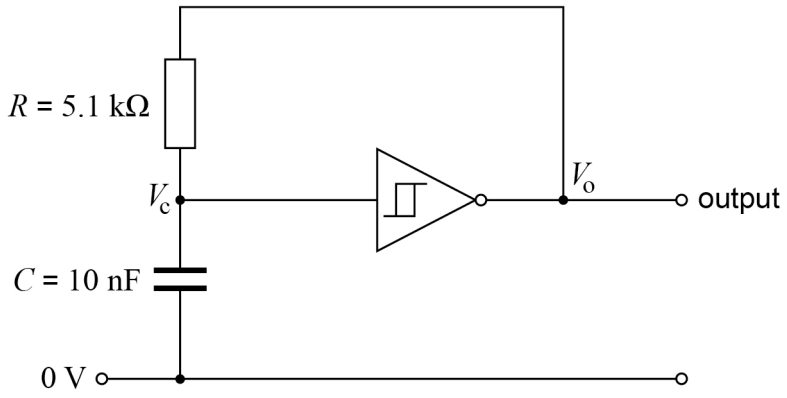
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ANSWER IN THE SPACES PROVIDED

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0 4 . 1 **Figure 6** shows an astable circuit based on a NOT logic gate. The symbol in the centre of the logic gate means that the output V_o changes at two different input values of V_c depending on whether the input voltage is rising or falling.

Figure 6



The pulse repetition frequency (PRF) for this particular circuit is given by:

$$\frac{1}{1.4\,RC}$$

Calculate the PRF in kHz

[1 mark]

PRF = _____ kHz

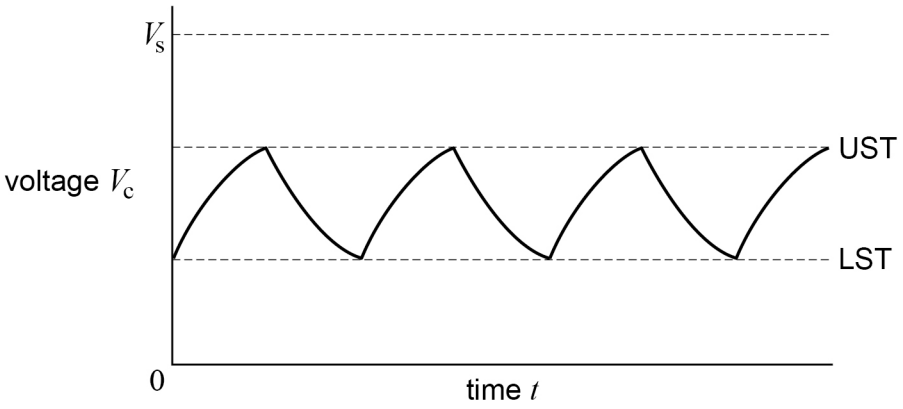
0 4 . 2 The supply voltage to the NOT gate is V_s

- When V_c increases and reaches the upper switching threshold (UST), the output of the NOT gate will switch from V_s to 0 V
- When V_c decreases and reaches the lower switching threshold (LST), the output of the NOT gate will switch from 0 V to V_s

The graph in **Figure 7** shows V_c constantly changing as the capacitor charges and discharges.

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Figure 7



Draw on **Figure 7** the output voltage V_o for the astable circuit.

[1 mark]

0 4 . 3 The circuit in **Figure 6** can be modified by the addition of a resistor to vary the PRF.

The astable is to be modified so that it produces a frequency 4 times that of the original.

Calculate the value of the resistor that should be added to the circuit and explain where in the circuit this additional resistor should be placed.

[2 marks]

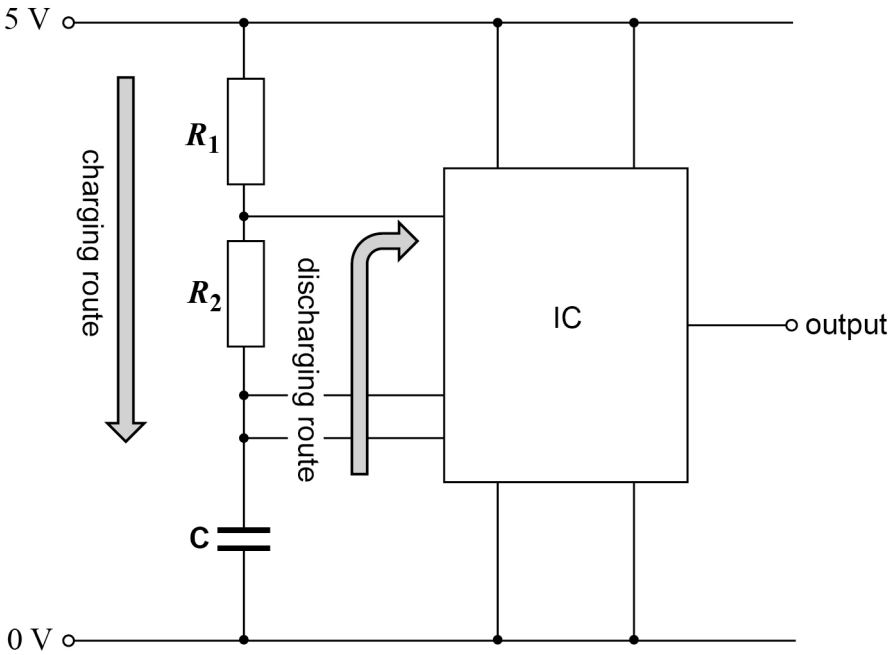
value of resistor = _____ kΩ

Question 4 continues on the next page

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0 4 . 4 In another astable, two resistors (R_1 and R_2) and a capacitor **C** form a timing chain to control the mark and space times for a square wave produced at the output of the integrated circuit (IC) shown in **Figure 8**.

Figure 8



The charging time for the capacitor **C** is: $t_C = 0.7 \times (R_1 + R_2) \times C$
The discharging time for the capacitor **C** is: $t_D = 0.7 \times R_2 \times C$

Calculate, in kΩ, values for R_1 and R_2 needed to produce a 5 kHz signal with 75% duty cycle given that the capacitor **C** has a value of 10 nF

[2 marks]

R_1 = _____ kΩ

R_2 = _____ kΩ

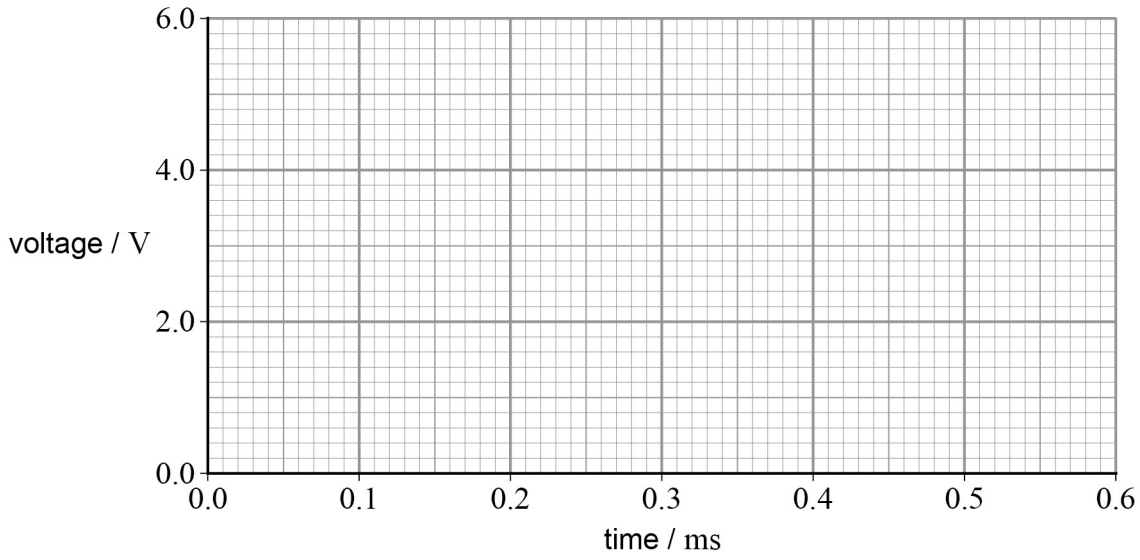
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0 4 . 5 The output of the IC in **Figure 8** is 5 V during the charging period and 0 V during the discharging period.

Draw on **Figure 9** the wave pattern that represents this signal.

[2 marks]

Figure 9



8

Turn over for the next question

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0 5 In a recording studio the output from a microphone is an analogue signal.
The equipment in the studio converts this analogue signal into a digital signal before storing it.

Discuss aspects of the analogue-to-digital conversion in this context.

In your answer you should include:

- what is meant by quantisation
- factors that affect the quality of the digital version of the analogue signal
- the advantages and disadvantages of digitising the analogue signal.

You may use diagrams to help make clear aspects of your answer.

[6 marks]

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END OF QUESTIONS

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